REMARKS

The Office Action dated March 31, 2005 has been carefully considered. Claims 1-17 are pending. The above amendments and following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1, 11 and 17 have been amended in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Claims 11 and 17 stand rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. Insofar as these rejections may be applied against the amended claims, they are deemed overcome. Claims 11 and 17 have been amended to describe "*generating an instruction-valid control bit.*" The language "detecting when valid instructions are not being executed by one or more stages by control logic" has been removed from Claims 11 and 17. Accordingly, Applicants respectfully request that the rejections of Claims 11 and 17 under 35 U.S.C. § 112, first paragraph, be withdrawn and that amended Claims 11 and 17 be allowed.

Claims 1-3 and 8 stand rejected under 35 U.S.C. § 102(e) in view of U.S. Patent 6,611,920 to Fletcher et al. ("Fletcher"). Insofar as these rejections may be applied against the amended claims, they are deemed overcome.

Claim 1 has been amended to more specifically recite one of the distinguishing characteristics of the present invention. The microprocessor contains "control logic that is at least configured to generate at least one instruction-valid control bit, wherein the at least one instruction-valid control bit is configured to *selectively* disable *only the* first clock derived from the main processor clock if a first stage is unused or to disable *only the* second clock derived from the main processor clock if a second stage is unused." Support for this amendment can be found, among other places, page 6, lines 10-15, of the original Application.

Fletcher does not suggest, teach, or disclose this feature of the present invention. Specifically, Fletcher discloses a conventional pipeline such that when data is latched a valid bit is simultaneously propagated through the clock generation logic to provide a clocking signal at each successive stage. In Fletcher the valid bit causes the clock generation logic to provide a clocking signal to every functional unit block. The present invention does not simply utilize a pipeline to propagate a valid bit. In contrast with Fletcher, a separate instruction-valid bit is generated for each stage. As shown in FIGURE 2 of the original Application, the control logic controls the instruction-valid bit(s), such that the first clock *or* the second clock can be disabled, independently. Accordingly, for example, a stop control signal can disable the first clock and a separate stop control signal can disable a second clock. This provides the present invention the ability to terminate data propagation through the stages at any time, and the ability to allow a clocking signal to be provided at each stage. These features allow the microprocessor to have increased the flexibility o to control the local clocks, which also improves the ability to test the stages.

The additional language in amended Claim 1 was added to clarify this feature of the present invention. Applicants respectfully submit that the ability to disable the first clock *or* the second clock is not disclosed in the Fletcher reference. Accordingly, the ability to *selectively* disable *only* the first clock or to disable *only* the second clock further distinguishes the present invention from Fletcher.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach, or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is both clearly and precisely distinguishable over the cited reference in a patentable sense. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 102(e) in view of Fletcher be withdrawn and that amended Claim 1 be allowed.

Claims 2-3 and 8 depend upon and further limit amended Claim 1. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 2-3, and 8 also be withdrawn.

Claims 4-7 and 9 stand rejected under 35 U.S.C. § 103(a) in view of Fletcher and U.S. Patent 6,304,125 to Sutherland ("Sutherland"). Insofar as these rejections may be applied against the amended claims, they are deemed overcome. Claims 4-7 and 9 depend upon and further limit amended Claim 1. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 4-7 and 9 also be withdrawn.

Claim 10 stands rejected under 35 U.S.C. § 103(a) in view of Fletcher and U.S. Patent 6,629,250 to Kopser ("Kopser"). Insofar as this rejection may be applied against the amended claims, it is deemed overcome. Claim 10 depends upon and further limits amended Claim 1. Hence, for at least the aforementioned reasons, this Claim should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejection of dependent Claim 10 also be withdrawn.

Applicants respectfully submit that independent amended Claim 11 is distinguished from the cited references for the same aforementioned reasons that amended Claim 1 is distinguished from the cited references. Specifically, the ability to *selectively* disable the first clock *or* the second clock is not disclosed by the cited references in any combination. Claims 12-16 depend upon and further limit amended Claim 11. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that amended Claims 12-16 be allowed.

Applicants respectfully submit that independent amended Claim 17 is distinguished from the cited references for the same aforementioned reasons that amended Claim 1 is distinguished from the cited references. Specifically, the ability to *selectively* disable the first clock *or* the second clock in an execution unit is not disclosed by the cited references in any combination.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-17.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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